APPLICATION NOTE

- TDA8798HL -
DUAL 8-BIT A/D CONVERTER WITH DPGA DEMONSTRATION BOARD

AN/99055

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DUAL 8-BIT A/D CONVERTER WITH DPGA
DEMONSTRATION BOARD

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SUMMARY

The **TDA8798** is a dual independent 8-bit **A**nalog-to-**D**igital **C**onverter with a dual **D**igitizing **P**rogrammable **G**ain **A**mplifier designed to read digital data storage and to be used for other applications. Each ADC converts the analog signal from the DPGA or from an other source (when the DPGAs is not used and disabled) into 8 bits binary digital words at a maximum sampling rate of 100 **M**ega **s**amples **p**er **s**econd. When it is used, each DPGAs controls the gain of input analog signals at a maximum amplification of 34dBv which is programmed by a manual digital serial interface or by a software. An external filter can be introduced between each DPGA and ADC.

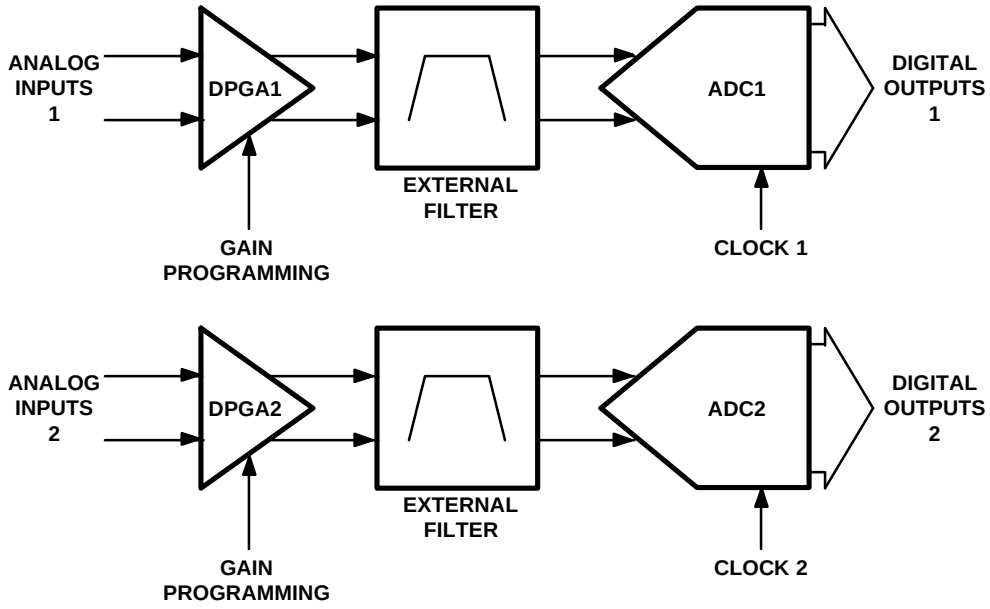
Only one version of this device exists: it is the **TDA8798HL** with clock frequency of 100Msps.

This **A**pplication **N**ote describes the design and the realisation of the **Demonstration Board** (n° 719) using the **TDA8798HL** version with an example of application environment.

To program the DPGAs from a **P**ersonal **C**omputer with Windows™ 3.1 and Windows™ 95, this **A**pplication **N**ote is associated with a **Demoboard/PC interface** software. The DPGAs can be programmed by a manual interface which is on the **Demoboard**.

1. MAIN FEATURES OF THE TDA8798HL:

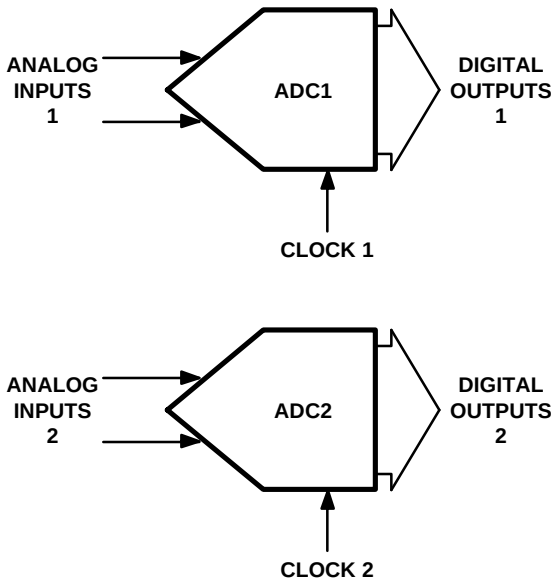
The **TDA8798HL** contains two channels, each made of one 8-bit **A**nalog-to-**D**igital **C**onverter and one **D**igital **P**rogrammable **G**ain **A**mplifier. A representation is given on **Figure 1**.



- Figure 1.Channels configuration -

These **ADC**s convert an analog input signal from DPGA into 8 bits binary coded digital words at a maximum sampling rate of 100Msps. These **DPGA**s control the gain of the analog signal between 0dBv and 34dBv.

The TDA8798HL can be used of single dual ADC converters which one representation is given on **Figure 2**.

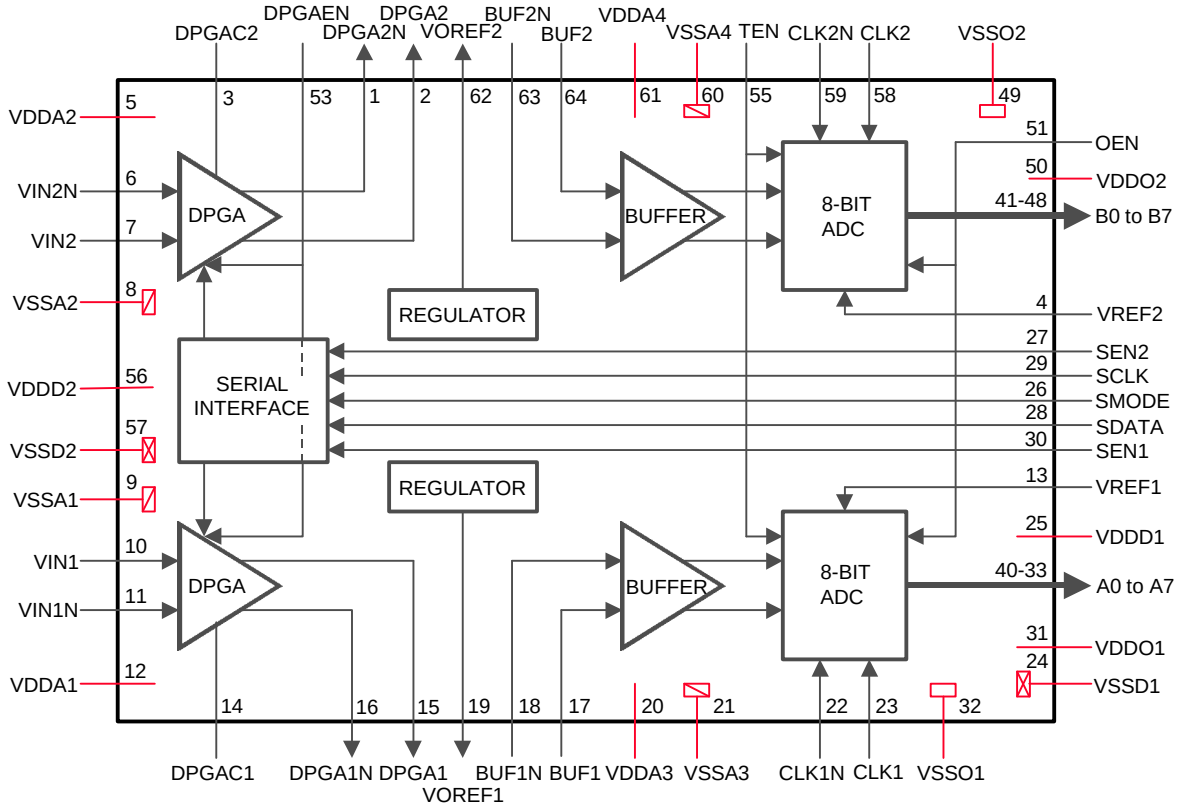


- Figure 2. Single dual ADCs configuration -

In this configuration, these **ADC**s convert an analog input signal into 8 bits binary coded digital words.

The **TDA8798HL** is supplied with 3.3V and the typical power dissipation is 327mW and is 465mW with DPGA enabled. The block diagram and the main specifications points of the **TDA8798HL** device are shown on **Figure 3**.

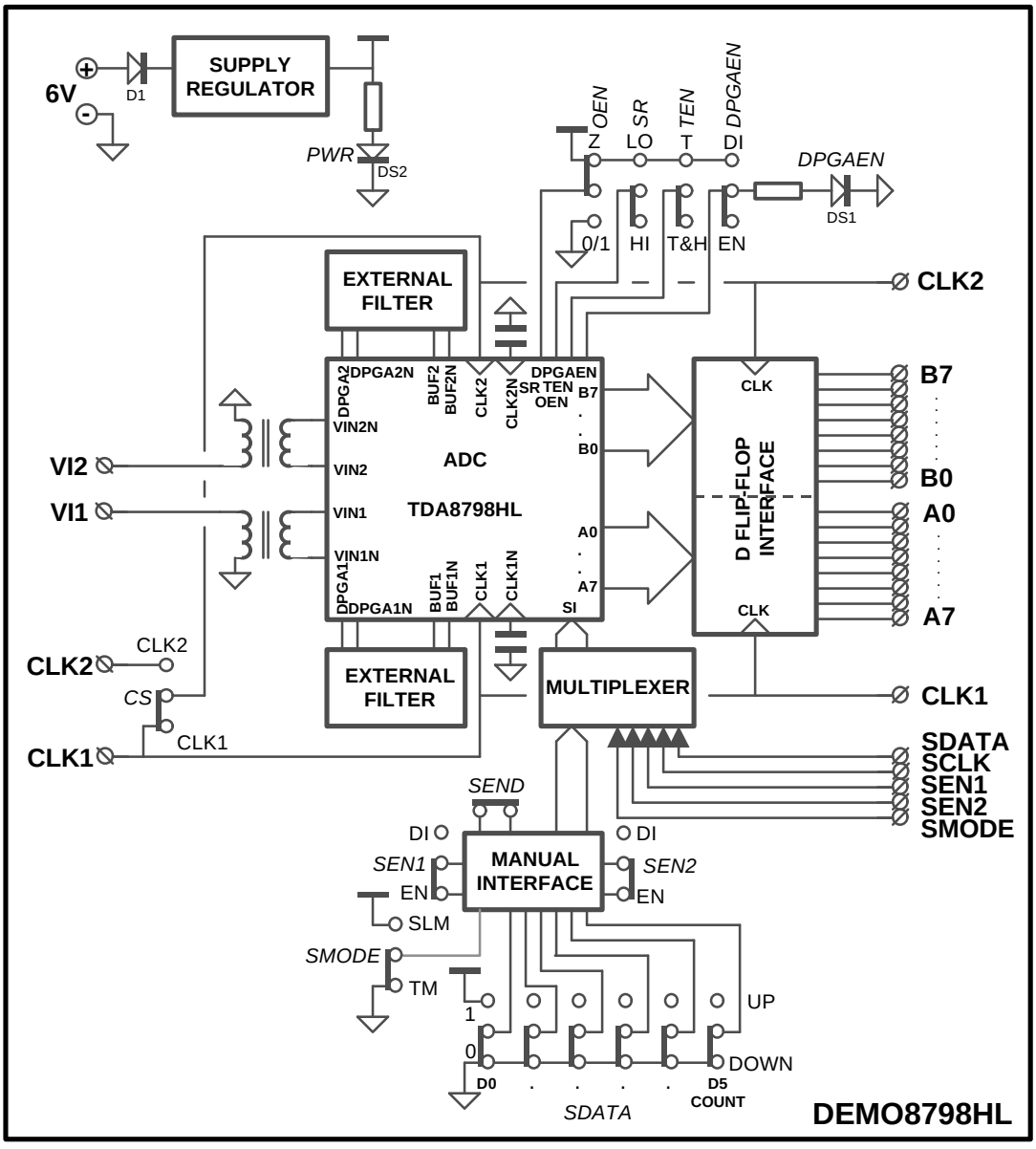
- Clock frequency: 100Msps.
- Power dissipation (typical): 327mW (DPGA disabled).
  465mW (DPGA enabled).
- ADC Accuracy: 8-bit.
- DPGA: 0dBV - 34dBv (on 6 bits).
- Supply: 3.3V.
- Compatibility: input/output: TTL and CMOS (3.3V).



- Figure 3. TDA8798HL block diagram -

2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board**, which is described in this **A**pplication **N**ote, is shown on **Figure 4**.



- Figure 4. Functional block diagram of the Demoboard -

The different blocks of the **Demoboard** are:

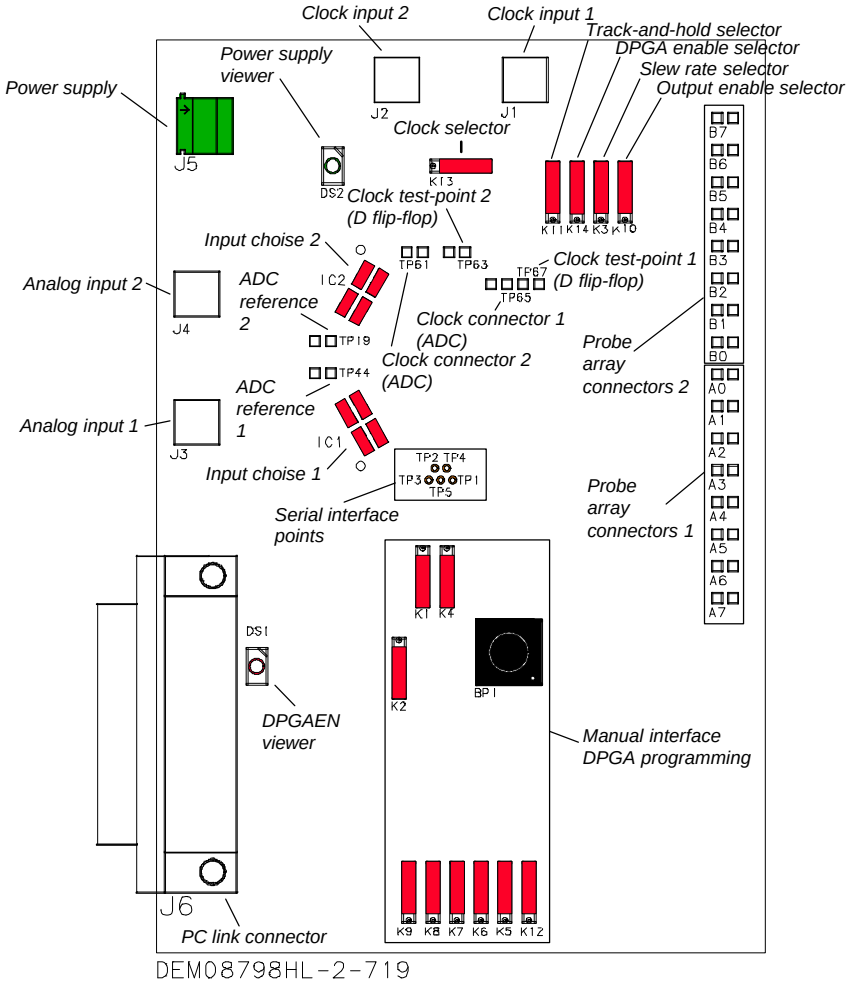
- A power **supply regulator** using to supply all circuitry on the board.
- An **external filter** improving the signal from DPGA for each channel when it is used.
- A **D flip-flop interface** synchronizing the ADCs data output.
- A **manual interface** programming by means of switches the gains of the DPGAs.
- A **multiplexer** choosing automatically either the manual programming from the manual interface or from the software programming the DPGAs gains.

The **Demoboard** works with a single $+6V_{DC}$ external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by a green LED.

The sampling clock signal on the **Demoboard** is available by plugging the 50Ω square generator in the CLK1 or/and CLK2 SMA connector(s).

3. OVERVIEW OF THE BOARD:

The whole implantation of this **Demoboard** is shown on **Figure 5**.



- Figure 5. Overview of the Demoboard -

The push-button and the different connectors, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J5** for **$6V_{DC}$** and **GND**.
2. A **PWR** green light **DS2** to indicate the good supply plugging.

- **For the evaluation of the TDA8798HL:**

1. Two SMA **J3** and **J4** connectors with 50Ω for the two DPGA analog input signals **VI1** and **VI2**.
2. Two SMA **J1** and **J2** connectors with 50Ω for the external clock inputs **CLK1** and **CLK2**.
3. A **CS** switch **K13** to choose a same clock or two different clocks for channels.
4. A switch **K10** to enable the ADCs outputs by the input **OEN**.
5. A switch **K11** to choose the track mode or the track & hold mode **TEN** of the two ADCs input analog signals.
6. A switch **K14** to enable or to disable the DPGAs by the input **DPGAEN**. When the DPGAs are disabled the **DPGAEN** red light **DS1** switch on.
7. A switch **K3** to control the slew-rate.
8. Two test-points **TP44** and **TP19** to control or to modified the ADC1 reference **VREF1** and the ADC2 reference **VREF2**.
9. Two input choice blocks **IC1** and **IC2** to use the ADCs with or without DPGAs.
10. Five points:
    TP3 to control the serial interface mode **SMODE**.
    TP1 to control the serial interface 1 enable **SEN1**.
    TP2 to control the serial interface 2 enable **SEN2**.
    TP4 to control the serial interface clock input **SCLK**.
    TP5 to control the serial interface data input **SDATA**.

- **For the reconstruction of the analog input waveform:**

1. Two eight-probe array connectors corresponding to the ADC1 digital output **A0** to **A7** and ADC2 digital output **B0** to **B7** are available to connect the logic analyser which computes the data.
2. Two connector **TP65** and **TP61** corresponding to the ADC1 and ADC2 clocks.
3. Two test-point **TP67** and **TP63** corresponding to the D flip-flop interface clocks.

- **For the manual programming of the DPGAs gains:**

1. A switch **K2** to choose the serial interface mode **SMODE** between the **S**erial **L**oad **M**ode and the **T**racking **M**ode.
2. A switch **K4** to enable/disable the serial interface 1 **SEN1**.
3. A switch **K1** to enable/disable the serial interface 2 **SEN2**.

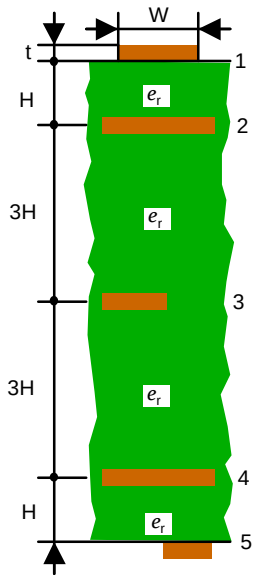
4. Six switches **K5** to **K9** and **K12** to program the serial interface data input **SDATA** in **SLM** mode. The switch **K12** is also used to choose the count-**UP** or the count-**DOWN** in **TM** mode.
5. A push-button **BP1** to send to DPGA the programmed gain.

- **For the gain software programming:**

1. A sub-d25 connector **J6** to plug the cable from the compatible PC computer using the gain programming software.

4. PCB DESIGN:

The design was made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 6**.



- Figure 6. PCB structure -

Five physical copper layers are used. The first and fifth layers are the signal layers which contain the microstrip lines. The second and fourth layers constitute the ground planes corresponding to signal layers. The third layer is designed specially for the power supply wires.

The metallized hole technique is employed to make all the necessary interconnections between the layers. The dielectric substrate used is an Epoxy Glass resin with a relative permittivity ($\boldsymbol{e_r}$) of 4.7 and a copper thickness (**t**) of 35µm (≈1.4mils). The substrate thickness (**H**) is ≈0.2mm (8mils) between the copper layers.

4.1 MICROSTRIP LINES:

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation is used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r+1.41}}{87}}} - \frac{t}{0.8},$$

(Accurate to within 5% when $0.1 < \frac{W}{H} < 3.0$ and $1 < e_r < 15$).

hence:

W = 12.7mils/0.32mm,

where:

Zo = 50Ω,
t = 1.4mils/≈35µm,
H = 8mils/≈0.2mm,
e_r = 4.7.

4.2 POWER SUPPLY WIRE:

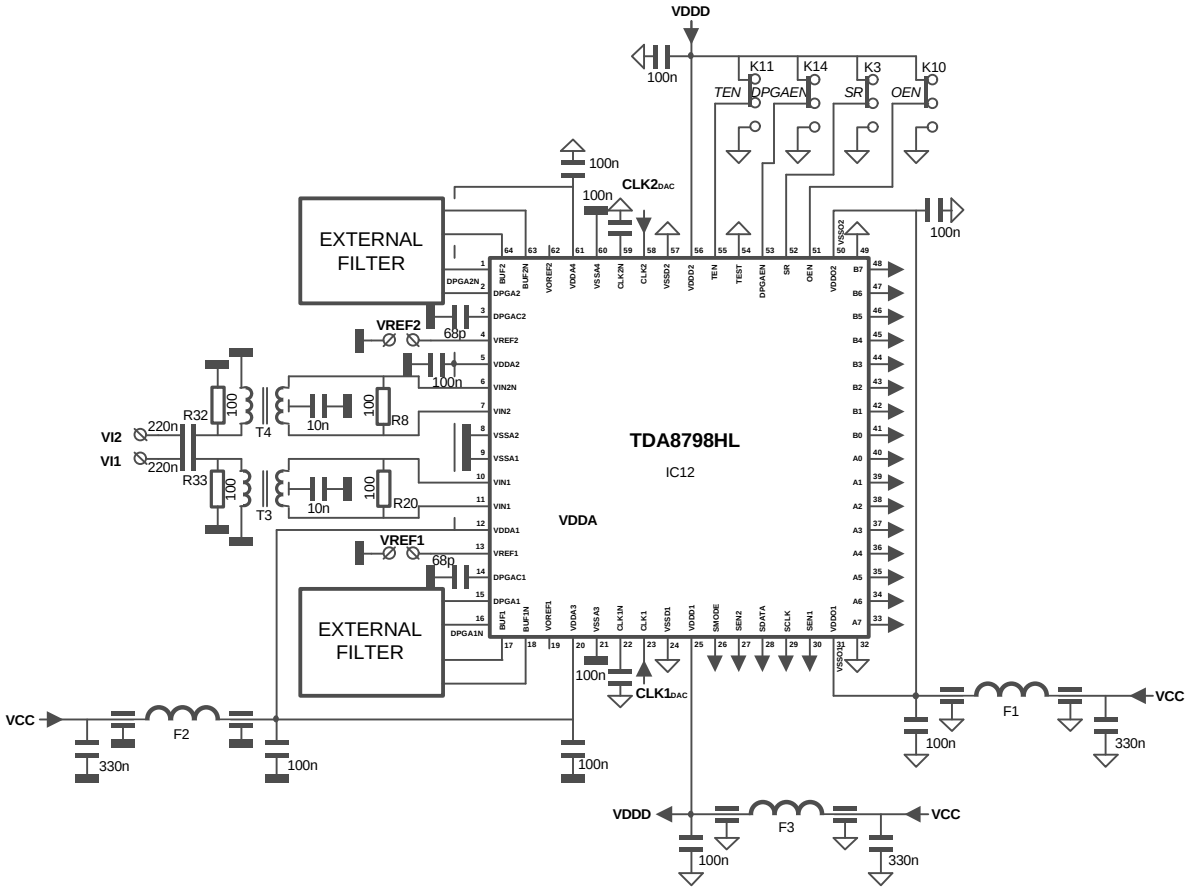
To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

4.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimise the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separated ground planes are designed on layers and are connected together through an inductor.

5. SPECIAL FEATURES OF THE APPLICATION BOARD:

To obtain optimal performances, the recommended application diagram is given on **Figure 7**.



- Figure 7. Typical TDA8798HL application diagram -

Subsequently, only one channel is described but all descriptions are valid for the second channel.

5.1 DPGA ANALOG INPUTS VIN1:

The dynamic DPGA analog inputs **VIN1** and **VIN1N** are connected through a 1:1 RF wideband transformer and a 220nF AC coupling to the external generator by the **VI1** SMA connector. this connector is adapted by a 50Ω microstrip line and a 50Ω equivalent resistor ending.

The maximum peak-to-peak magnitude value $\mathbf{VI1_{p.-p}}$ of the dynamic input signal to obtain the full scale of DPGA analog outputs **DPGA1** and **DPGA1N** on the board is determined from the approximate relation:

$$VI1_{p.-p} = \frac{FS}{10^{\frac{G}{20}}},$$

where:

G: DPGA gain,
FS: DPGA output full scale (0.5V),

hence:

$\mathbf{VI1_{p.-p}} \approx \mathbf{10mV}$ at G_{max} = 34dBv,

(corresponding at $5mV_{p.-p}$ on each input **VI1** and **VI1N**),

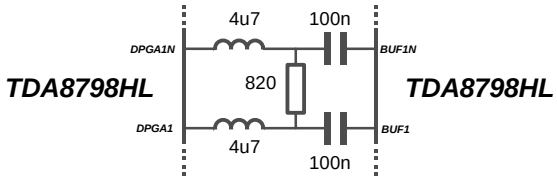
and:

$\mathbf{VI1_{p.-p}} = \mathbf{0.5V}$ at G_{min} = 0dBv.

The DPGA mode DPGAEN is chosen with the switch **K14**. When the DPGA is disable, the **DPGAEN** red light **DS1** is alight.

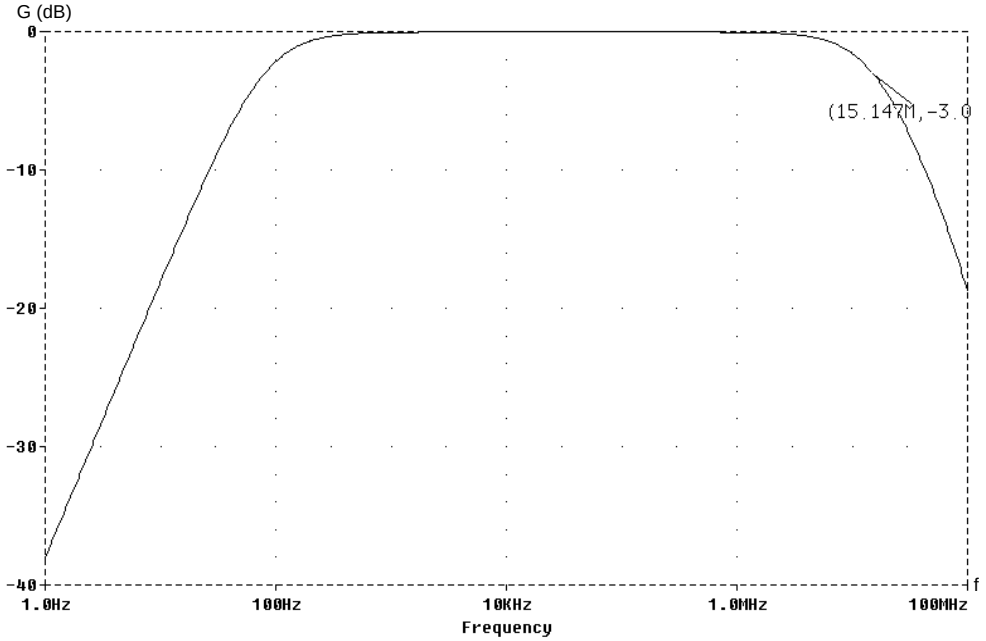
5.2 EXTERNAL FILTER:

A bandpass filter (typical application) is connected between the differential DPGA outputs **DPGA1** and **DPGA1N** and the differential ADC inputs **BUF1** and **BUF1N**. The diagram of this filter is shown on **Figure 8**.



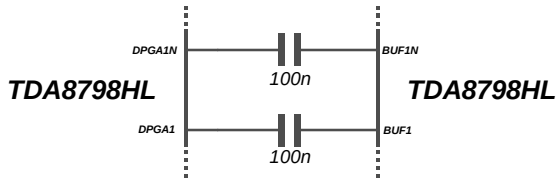
- Figure 8. Bandpass filter -

The simulated frequency response of this external filter example is shown on **Figure 9**.



- Figure 9. Gain response of this bandpass filter -

A capacitive link *can be connected between the differential DPGA outputs and the differential ADC inputs which diagram is shown on* ***Figure 10****.*



- Figure 10. Capacitive link -

5.3 ADC ANALOG INPUTS BUF1 AND BUF1N:

The dynamic ADC analog inputs are connected through an external filter or through something else to the DPGA outputs or to another analog source by the connector **J3**. The peak-to-peak magnitude nominal value $\mathbf{VI_{p.-p}}$ of the dynamic input signal is 500mV corresponding to 250mV on each analog input **BUF1** and **BUF1N**. The quantum of the **TDA8798HL** is defined by:

$$q = \frac{VI_{p.-p}}{2^8 - 1},$$

hence,

$$\mathbf{q \approx 2mV}.$$

The full scale of ADC input can be changed to force a voltage on ADC1 reference **VREF1** test point **TP44**. The approximate relation between this reference and the ADC full scale inputs is given by:

$$FS = 0.416 \times VREF1 - 0.04,$$

where:

$$VREF1 \in [1;2.5].$$

When the VREF1 is forced by an external voltage, the performances of ADC are changed and not guaranteed.

The track & hold mode **TEN** is chosen with the switch **K11**.

5.4 DATA OUTPUT A0 TO A7:

All data outputs of the **TDA8798HL** are TTL/CMOS compatible and they are directly addressed to a D-flip flop interface circuit.

The switch **K10** connected to the **OEN** pin allows either to active the data outputs or to disactive on them.

The switch **K3** connected to the **SR** pin allows to change the edge of slew rate (to have more current on outputs).

5.5 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLY:

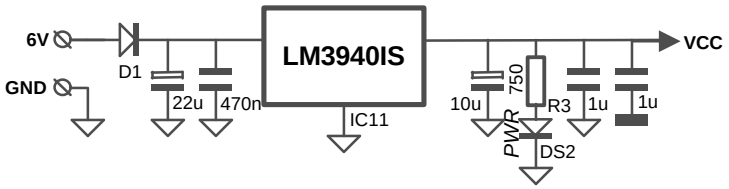
A single power line of 3v3 is used to supply the TDA8798HL and all circuits on **Demoboard**.

To ensure a good bypassing at low and high frequencies, the use of several different parallel capacitors was required and SMD bypass π type filters are implanted on the board near the ADC.

6. ENVIRONMENT CIRCUITS:

6.1 GENERAL POWER SUPPLY:

The electrical diagram is shown on **Figure 11**. An external DC power unit of $6V_{DC}$/280mA is used to supply the **Demoboard** across the diode **D1**.

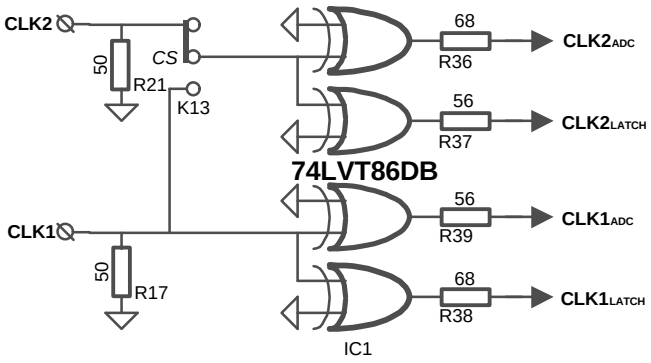


- Figure 11. Electric diagram of the power supply -

The BYD17G silicon diode **D1** ensures the protection of all the circuitry from reverse polarities. The good supply plugging is indicated by the **PWR** green LED **DS2**.

6.2 EXTERNAL CLOCK SELECTOR:

On the **Demoboard**, the **CLK1** connector **J1** allows to drive the ADC1 and a part of D-type flip-flop circuit. The **C**lock **S**elector switch **K13** allows to drive the ADC2 and the other part of D-type flip-flop circuit either from the **CLK1** or form an other source connected through the **CLK2** connector **J2**.
To synchronise all clocks on the demoboard, a SMD IC exclusive-or gate **74LVT86DB** from the Low Voltage Technology logic family of PHILIPS SEMICONDUCTORS is used . The electric diagram of external clock selector is given on **Figure 12**.



- Figure 12. Electric diagram of the clock selector -

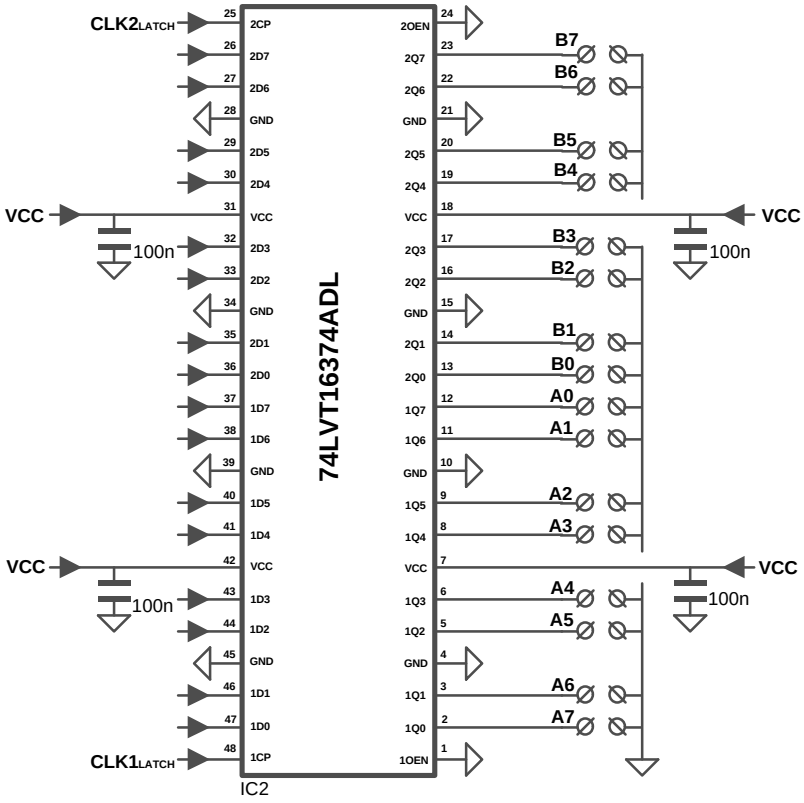
The **R36**, **R37**, **R38** and **R39** resistors are used to improve the clock signal.

Advice:

Usually, in some applications where the clock signal is not adapted, it is necessary to put a resistor, for of the ADC clock input, on the clock signal line. This resistor allows to eliminate principaly the undershoot and to improve the clock signal.

6.3 D-TYPE FLIP-FLOP INTERFACE:

The electric diagram of the latch interface is shown on **Figure 13**. It allows to recover each ADC data outputs synchronized on the clock sampling.

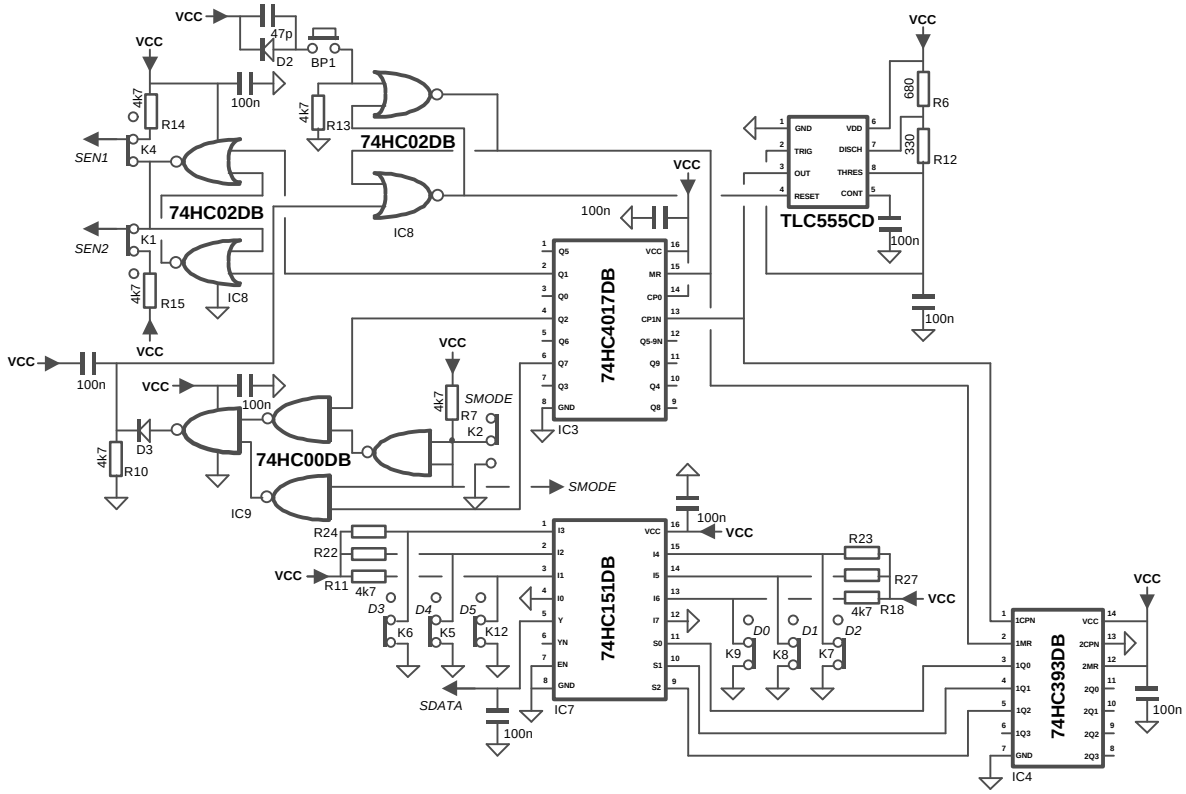


- Figure 13. Electric diagram of the D-type flip-flop interface -

The interface circuit uses a SMD ICs edge-triggered D-type flip-flop **74LVT16374ADL** of the Low Voltage Technology logic family.

6.4 MANUAL INTERFACE:

The electric diagram of the manual interface is shown on **Figure 14**. This interface allows to program the DPGAs registers without the use of the software supplied with the **Demoboard**.



- Figure 14. Electric diagram of the manual interface -

The push-button SEND sets the R-S bistable made with two gates of **IC8**. In this state, this bistable enables the clock of the interface made from the **IC10** timing circuit. This clock, corresponding with **SCLK** signal, goes into the **IC3** Jonhson decade counter and the **IC4** binary ripple counter.
The **IC3** Jonhson decade counter allows to set the SEN1 and SEN2 or the both across the R-S bistable made with the two other gates of **IC9**, and to reset across the **IC9** glue logic the manual interface after two clock cycle corresponding to **T**racking **M**ode or after seven clock cycle corresponding to **S**erial **L**oad **M**ode.
The **IC4** binary ripple counter is used to control the **IC7** 8-input multiplexer which translate the parallel word, programmed with the switches **K5** to **K9** and **K12**, into **SDATA** serial word. To avoid of noise on

the **Demoboard**, the clock manual interface signal is enable only when the data is send into **TDA8798HL** circuit.
The manual interface uses several SMD ICs of the High-speed CMOS logic family of PHILIPS SEMICONDUCTORS.

The push-button and the different switches available on the manual interface are:

- The switch **K2** corresponding to the **SMODE** is used to choose the mode of programming:
    1. The **SLM** mode corresponding to the **S**erial **L**oad **M**ode, allowing to program directly the DPGAs registers.
    2. The **TM** mode corresponding to the **T**racking **M**ode, allowing either to increase or to decrease the DPGAs registers values by 0dBv54 steps. **In this mode, it is recommended to set on 0 from K5 to K9 switches**.

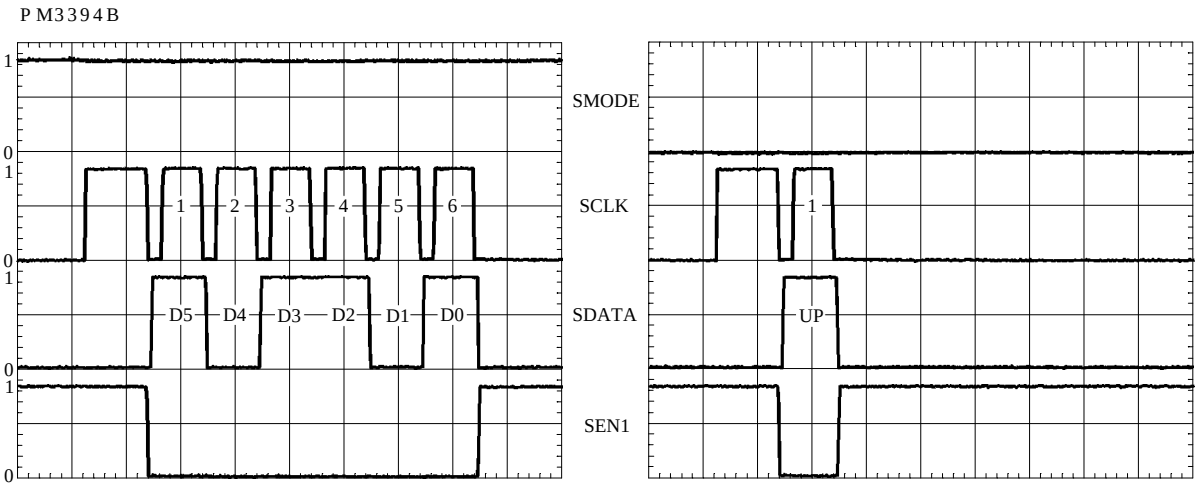
- The switches **K4** and **K1** corresponding to **SEN1** and **SEN2** are used to enable or disable the DPGA registers accesses.

- The switches **K5** to **K9** corresponding to the **SDATA** are used to program the 6-bit word to send to the DPGAs registers in **SLM** mode.

- The switch **K12** also corresponding to the **SDATA** is used to program the increase or the decrease the DPGAs registers in **TM** mode.

- The push-button **BP1** is used to send the **SDATA** from the **K5** to **K9** and **K12** switches into DPGAs registers.

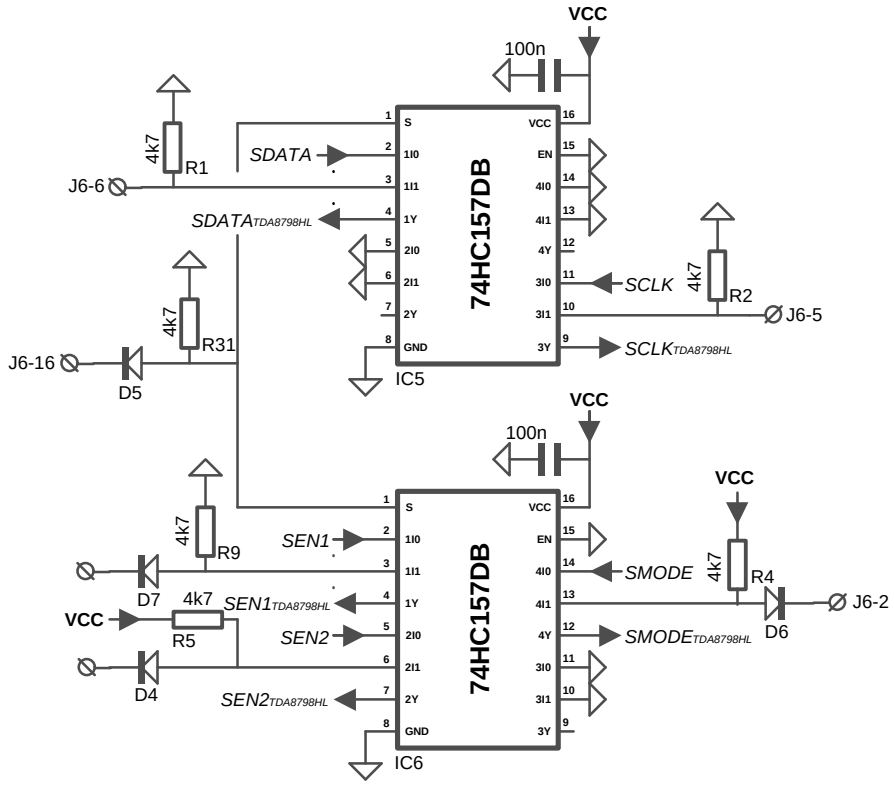
The waveforms of **SDATA**, **SMODE**, **SEN1**, **SEN2** and **SCLK** are given on **Figure 15**.



- Figure 15. Waveforms from manual interface -

6.5 MULTIPLEXER:

The electric diagram of the multiplexer allowing to commute between the manual interface and the Demoboard/PC interface is given on **Figure 16**.



- Figure 16. Electric diagram of the multiplexer -

The interface circuit uses two SMD ICs quad two-input mutliplexer **74HC157DB** of the High-speed CMOS logic family of PHILIPS SEMICONDUCTORS.

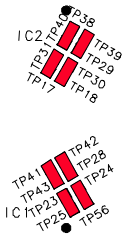
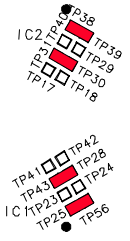
When a sub-d25 cable is connected between the **Demoboard** and the PC parallel port, and when the interface software is run, the manual interface is automatically disabled.

7. OPERATING MODE:

A external power unit of 6V/280mA is required to supply the **Demoboard**. However, the board is able to work until 9V.

7.1 INPUT OPERATION:

The **I**nput **C**onfiguration block allows to configure the working mode of the Demoboard. Referring to the **Table 1** to select the appropriate mode.

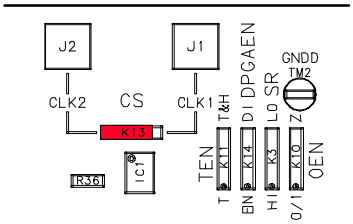
Mode	Function	Jumpers position	Note
0	The DPGA's and the ADC's are used.		The **DPGAEN** switch **K14** must be at **EN**able (the LED **DS1** is off).
1	The ADC's are used and the DPGA's are disabled.		The **DPGAEN** switch **K14** must be at **Di**sable (the LED **DS1** is on)

- Table 1. Mode and jumpers position -

7.2 SINGLE CLOCK MODE:

In this mode, an external 50Ω square clock generator is used for two ADC's. The position of the switch and the location of the connector are given on **Figure 17**. To use this mode, follow the instructions below:

- Put the **C**lock **S**elector to **CLK1** with the switch **K13**.
- Connect an external 50Ω square clock generator to the 50Ω SMA connector **J1**.



- Figure 17. Board configuration using the single clock mode -

The required clock levels are:

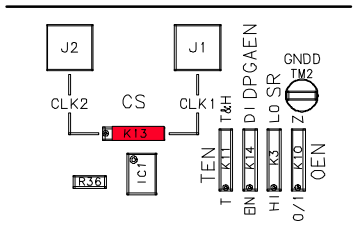
V_{CLKH} min = 2.0V,

V_{CLKL} max = 0.8V.

7.3 DUAL CLOCK MODE:

In this mode, an external 50Ω square clock generator is used to each ADC. The position of the switch and the location of connectors are given on **Figure 18**. To use this mode, follow the instructions below:

- Put the Clock Selector **CS** to **CLK2** with the switch **K13**.
- Connect the first external 50Ω square clock generator to the 50Ω SMA connector **J1**.
- Connect the second external 50Ω square clock generator to the 50Ω SMA connector **J2**.



- Figure 18. Board configuration using the dual clock mode -

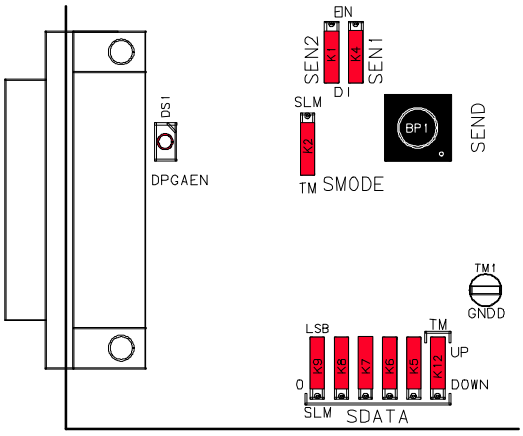
The required clock levels for all modes are:

$$V_{CLKH} \text{ min} = 2.0V,$$

$$V_{CLKL} \text{ max} = 0.8V.$$

7.4 DPGA MANUAL PROGRAMMATION (MODE 0 ONLY):

The location of the switches and push button is given on **Figure 19**. **The DPGAEN LED DS1 must be off otherwise put the DPGAEN switch at EN**.



- Figure 19. Board configuration using the manual interface -

To program the DPGAs registers from the manual interface, follow the instructions:

1. Choose the mode by **SMODE** with the switch **K2**. The modes are **T**racking **M**ode and **S**erial **L**oad **M**ode.
2. **EN**able or **DI**sable the register accesses by **SEN1** and **SEN2** with the switches **K4** and **K1**.
3. Program the data or the up/down by **SDATA** with the switches **K9**, **K8**, **K7**, **K6**, **K5** and **K12** or **K12** depending on the chosen mode.
4. Press the push-button **BP1** to send the **SDATA** value into **TDA8798HL** circuit.

7.5 DPGA DEMOBOARD/PC INTERFACE SOFTWARE (MODE 0 ONLY):

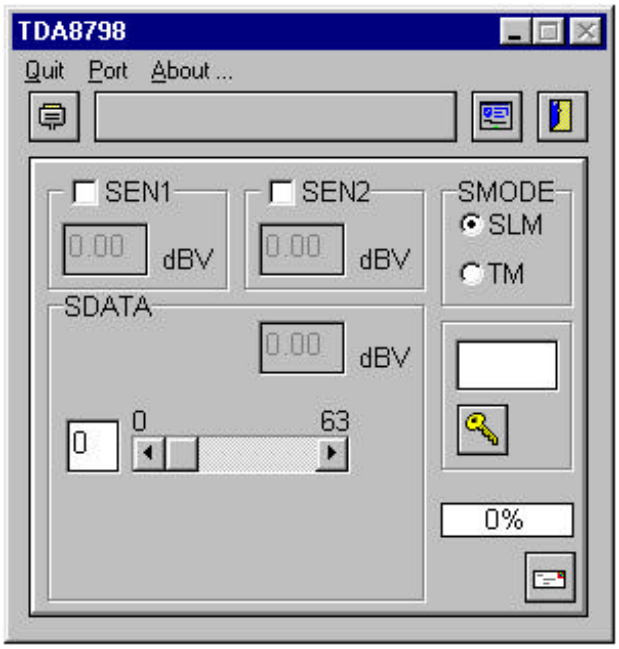
The **Demoboard/PC** interface software allows to change the values of DPGA gain control registers from a Personnel Computer. When the sub-d25 cable is connected between the **Demoboard** from **J6** connector to the PC parallel port and the interface software running, the manual interface is automatically disabled. **In this mode, The DPGAEN LED DS1 must be off**.

- **Install TDA8798HL software:**

To install the TDA8798HL software, a PC and Windows™ 3.11 or 95 are required. Then follow the instructions below:

1. Insert the **TDA8798HL Software** disk into appropriate disk drive of the computer.
2. Create a directory named **tda8798** under the hard disk. If needed, refer to the notice of Windows™.
3. Create the directory named **w311** under the **tda8798** directory.
4. Put all files of the TDA8798HL Software floppy disk into **c:\tda8798\w311** directory
5. Double click on the **tda8798.exe** file.

On the **Figure 20** is given the representative window after the running of the **tda8798** software.



- Figure 20. Main window of the Demoboard/PC interface software -

- **General use:**

The **Quit** menu allows to quit the program.

The **Port** menu, on **Figure 21**, allows to choose the LPT port. By default the LPT2 port is selected.

- Figure 21. Port menu -

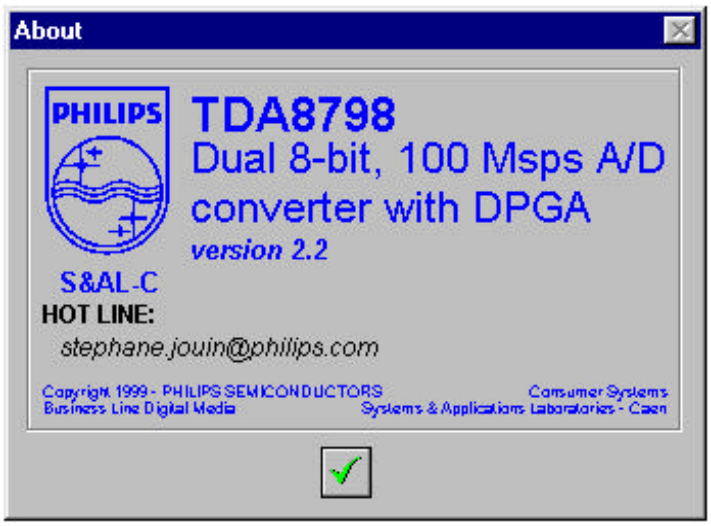
Lpt1: selects the LPT1 port.

Lpt2: selects the LPT2 port.

Lpt3: selects the LPT3 port.

Autodetect: search automatically the port on which is connected on the **Demoboard**.

The **About …** menu gives some information about the program and the support. A view of this window is given on **Figure 22**.



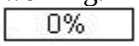
- Figure 22. About window -

- **Description:**

Some buttons and gauge are available on the main window:

 is the send button to send data into internal registers **DPGA1** or **DPGA2** or both of them.

 is the test mode button and it is reserved for the Philips test and it must not use it in standard working.



is the gauge. It shows the state of communication between the device and the PC. When the gauge returns to 0%, the communication is finished.

The two radio button () **SLM** and **TM** of **SMODE** allows to choose the programming mode. Tick the appropriate radio button to enable the **S**erial **L**oad **M**ode or the **T**racking **M**ode.

In **SLM** mode, an edit window () and a scroll bar () allows to introduce or to change the decimal value of **SDATA**. A grey edit window give the approximately corresponding value in dBv of **SDATA**.

In **TM** mode, two check buttons ( ) **UP** and **DOWN** of **SDATA** allow either to count up or to count down the internal registers **DPGA1** or **DPGA2** or both of them. The step of the count up or count down is given on the grey edit window.

The two check buttons **SEN1** and **SEN2** allow to enable or to disable the register 1 or the register 2 or the both of them. Tick the check button to enable the chosen registers. Two grey edit windows give the approximate value of the two registers.

- **Speed button:**

In the window, some speed buttons are available to access rapidly at some functions:

 detects automatically the good LPT port.

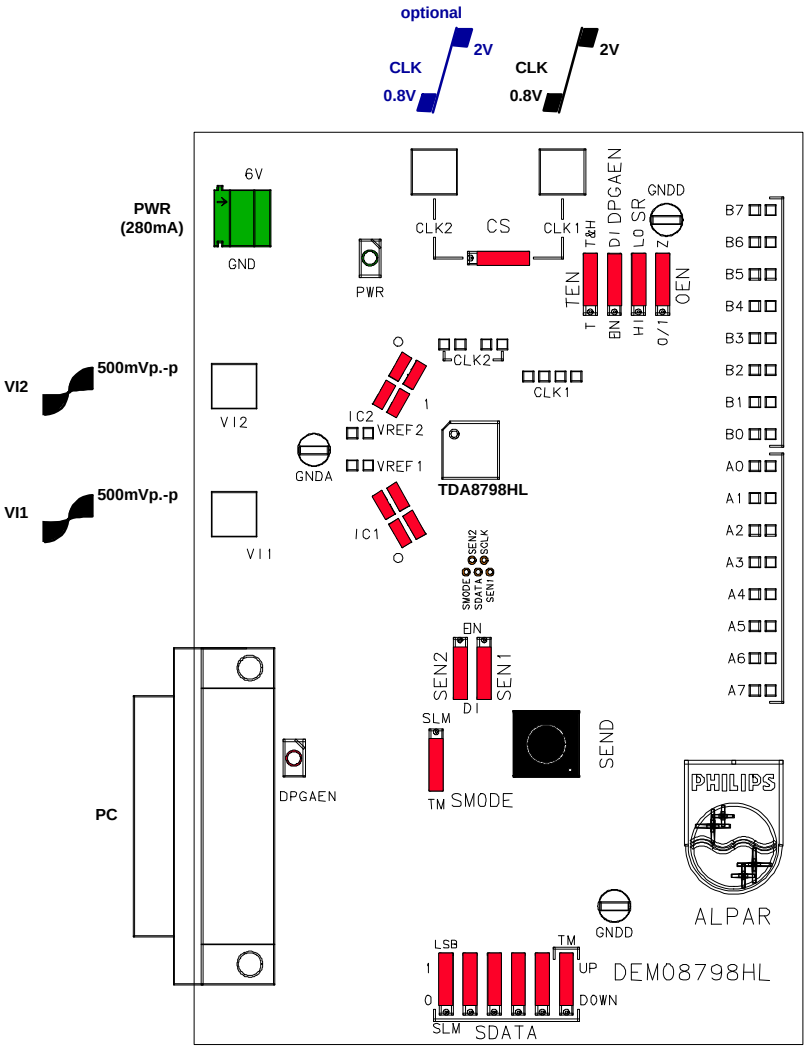
 accesses to the about window.

 allows to quit the program.

The Demoboard/PC interface software made under Windows™ 3.11 but it can run with Windows™ 95.

7.6 QUICKVIEW OF THE DEMOBOARD:

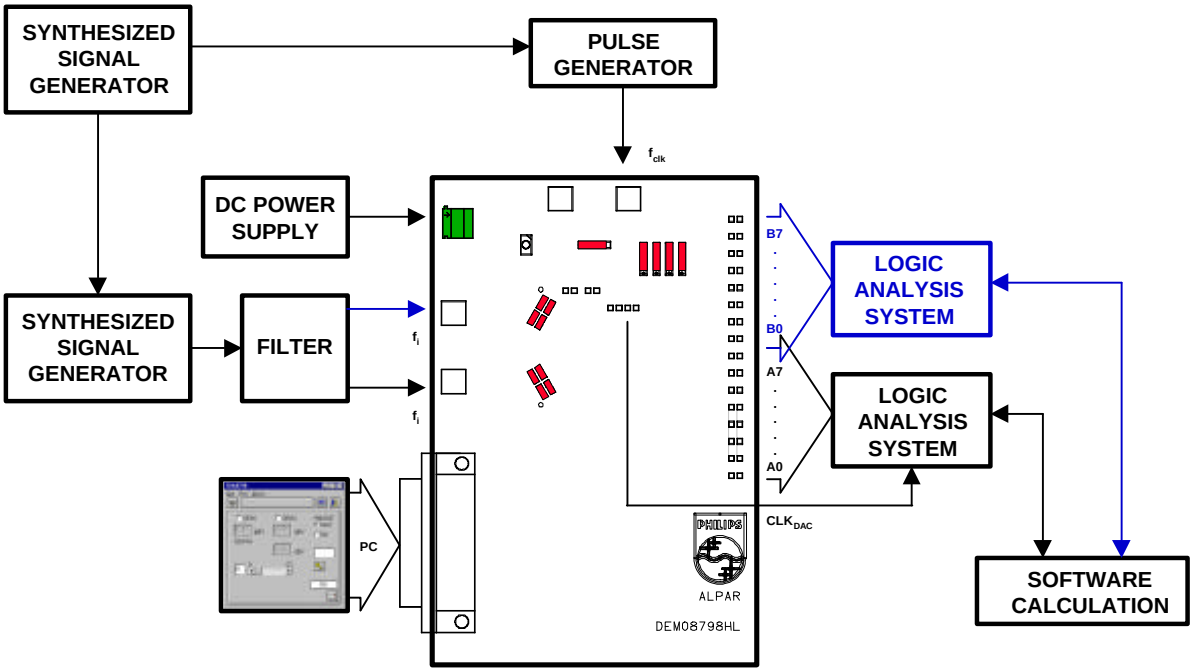
A quick view of the **DEMO8798** with main information is given on **Figure 23**.



- Figure 23. Quickview of the DEMO8798HL -

8. PERFORMANCES:

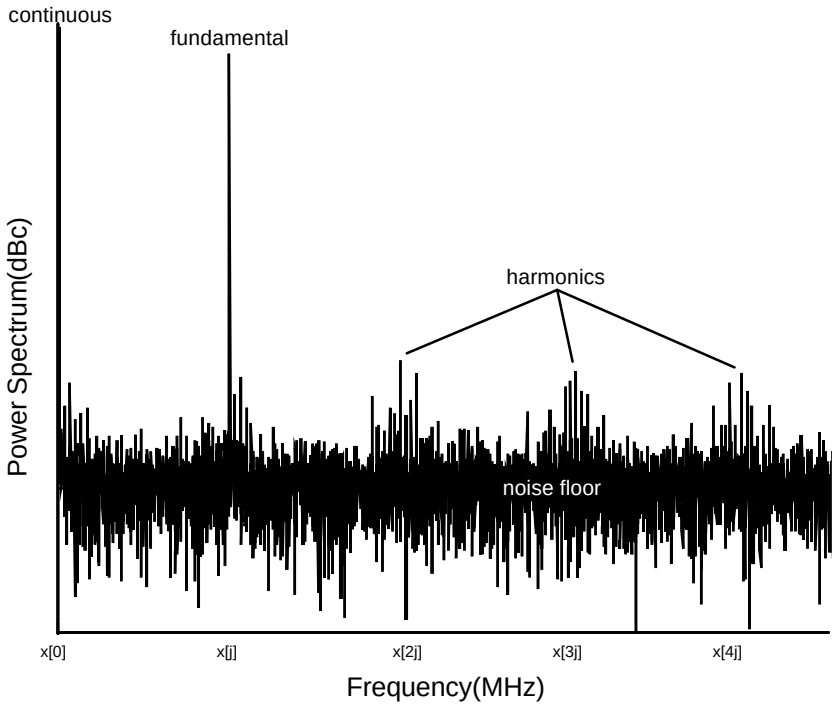
An evaluation of the performances of the **TDA8798HL** is made with the **Demoboard** environment on the CAEN dynamic bench at 100Msps which block diagram is given on **Figure 24**.



- Figure 24. CAEN's dynamic bench block diagram -

8.1 DEFINITION OF THE MEASURING PARAMETERS:

To evaluate the performances of ADC on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters from the sample signal.



- Figure 25. FFT -

According to the FFT shown on **Figure 25**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$THD_{dBc} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2}^{6} x^2[i \times j]}}.$$

Where:

x[j] : fundamental component corresponding with the j spectrum component,

x[i × j] : component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$SFDR_{dB} = 20 \times \log_{10} \frac{x[j]}{MAX(x[i])}.$$

Where:

$x[i]$: spectrum component i with $i \in [2:\frac{N}{2}]$ (N=8192: number of samples) and $i \neq x[j]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$SINAD_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j}^{\frac{N}{2}} x[i]}}.$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}}.$$

- the **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

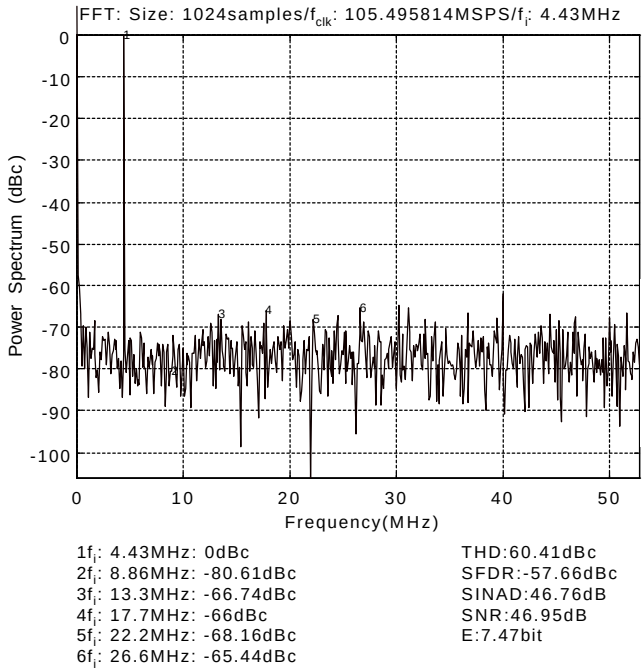
$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log_{10} 2}.$$

8.2 MEASUREMENT OF THE ADC 1 (MODE 1):

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	4.43MHz.
Waveform:	Sinus.
Magnitude:	Full Scale (FFT).
Antialiasing Filter:	Yes.
Clock frequency:	105Msps.
Operating mode:	External clock.

The typical results and corresponding diagram obtained with these conditions is shown on **Figure 26**.



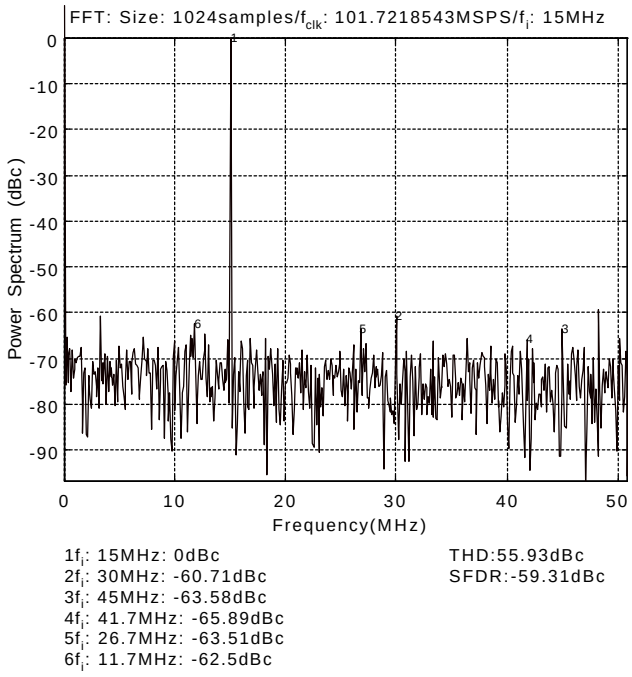
- Figure 26. FFT results of ADC 1 (mode 1) -

8.3 MEASUREMENT OF CHANNEL 1 (MODE 0) IN MINIMUM GAIN:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	15MHz.
Waveform:	Sinus.
Magnitude:	Full Scale (FFT).
Antialiasing Filter:	Yes.
Mode:	Track-and-hold.
Gain Register:	00h/0dBv.
Clock frequency:	101Msps.
Operating mode:	External clock.

The typical results and corresponding diagram obtained with these conditions is shown on **Figure 27**.



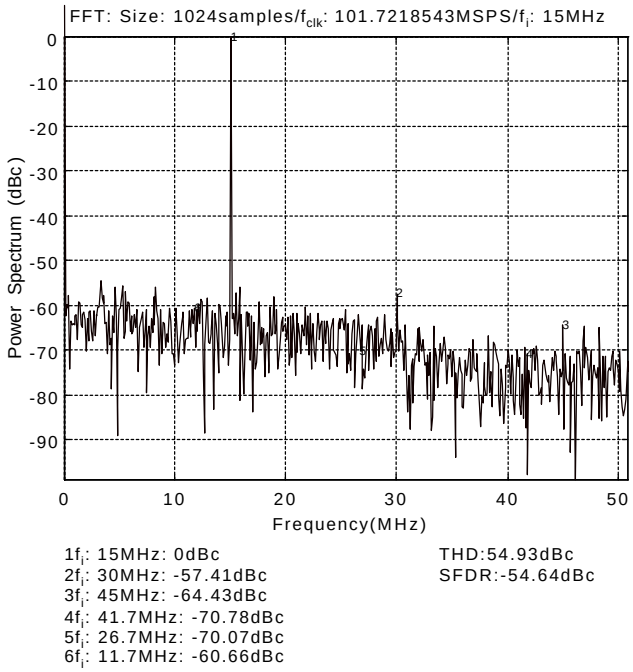
- Figure 27. FFT results of channel 1 (mode 0) in minimum gain -

8.4 MEASUREMENT OF CHANNEL 1 (MODE 0) IN MAXIMUM GAIN:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	15MHz.
Waveform:	Sinus.
Magnitude:	Full Scale (FFT).
Antialiasing Filter:	Yes.
Mode:	Track-and-hold.
Gain Register:	3Fh/34dBv.
Clock frequency:	101Msps.
Operating mode:	External clock.

The typical results and corresponding diagram obtained with these conditions is shown on **Figure 28**.



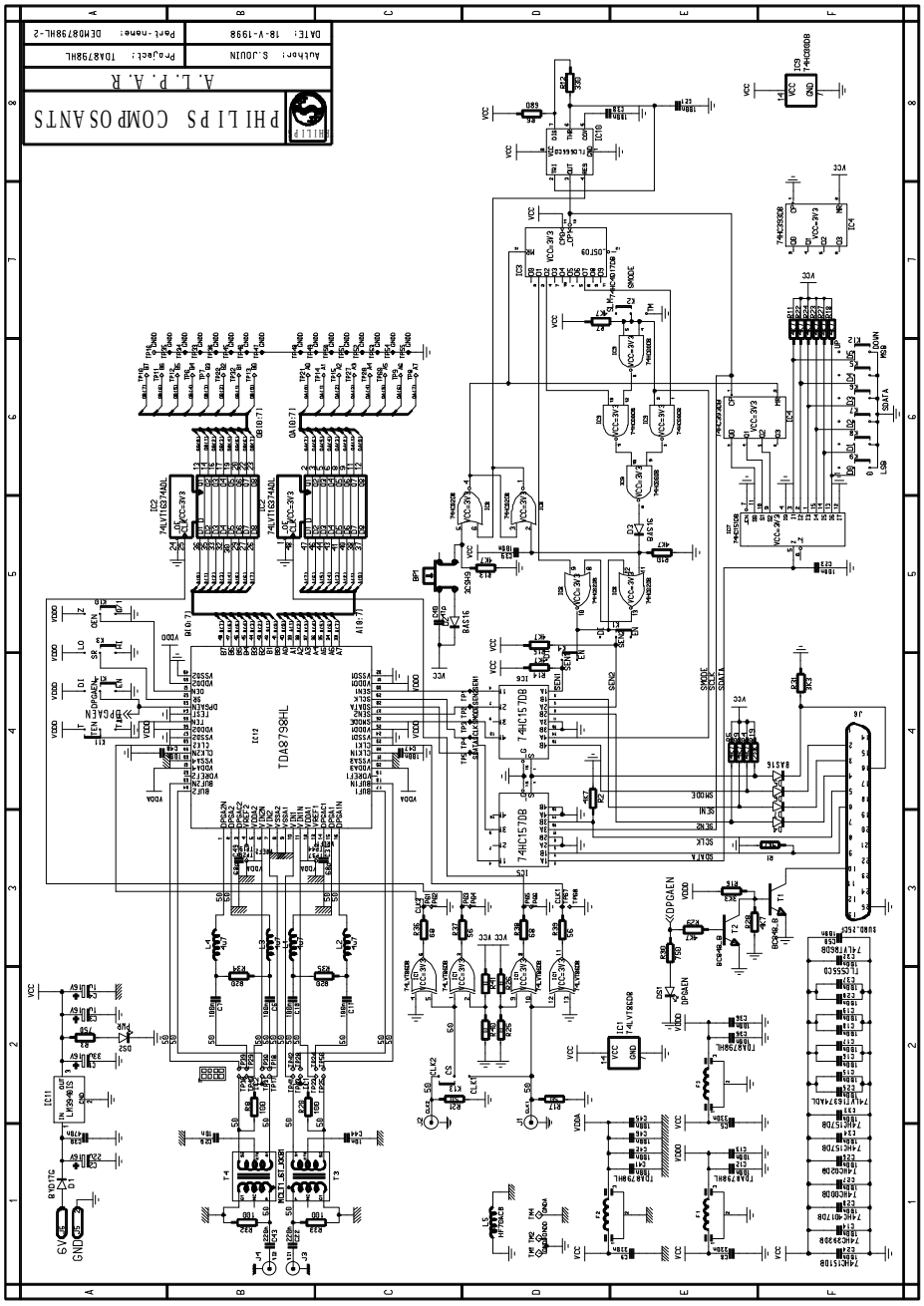
- Figure 28. FFT results of channel 1 (mode 0) in maximum gain -

9. DEMOBOARD FILES:

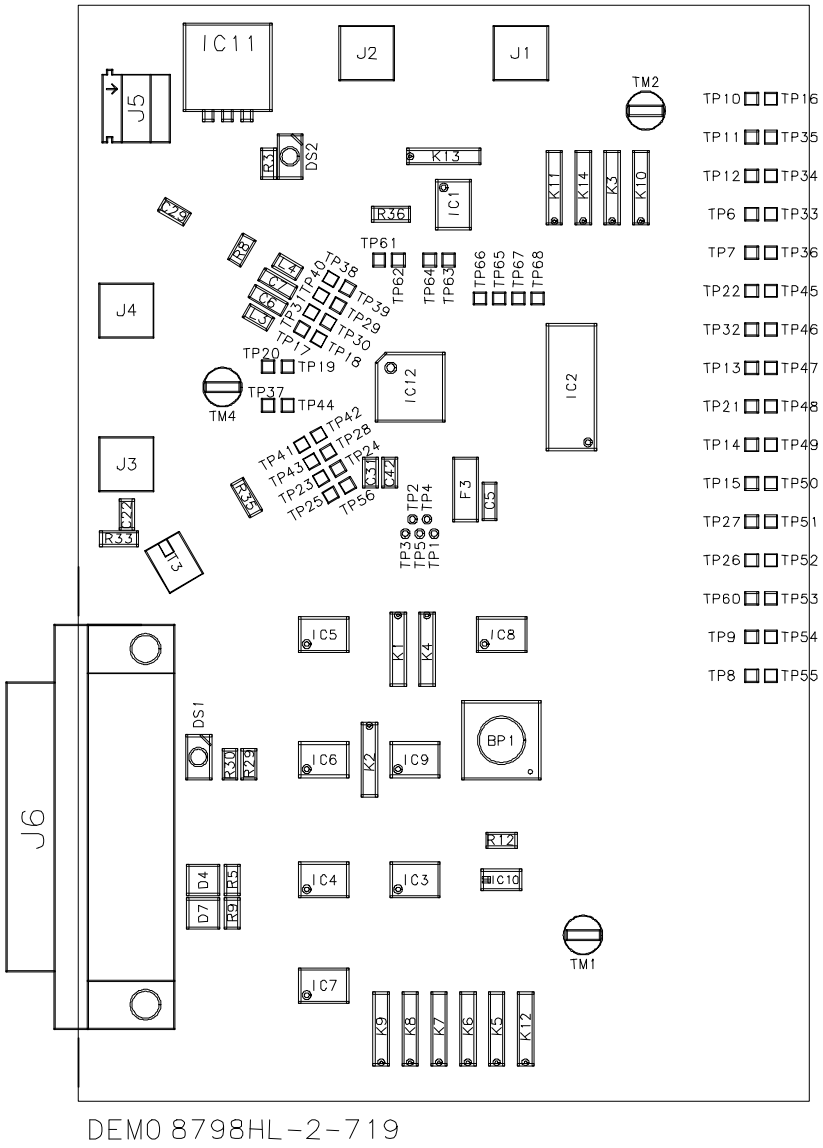
All documents needed for the realisation of this **Demoboard** are given from **Figures 29 to 36**.

- Electrical diagram.
- Silk-screen printing.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Internal layout ground layout 2.
- Internal layout supply layout 3.
- Internal layout ground layout 4.
- Underside component layout 5

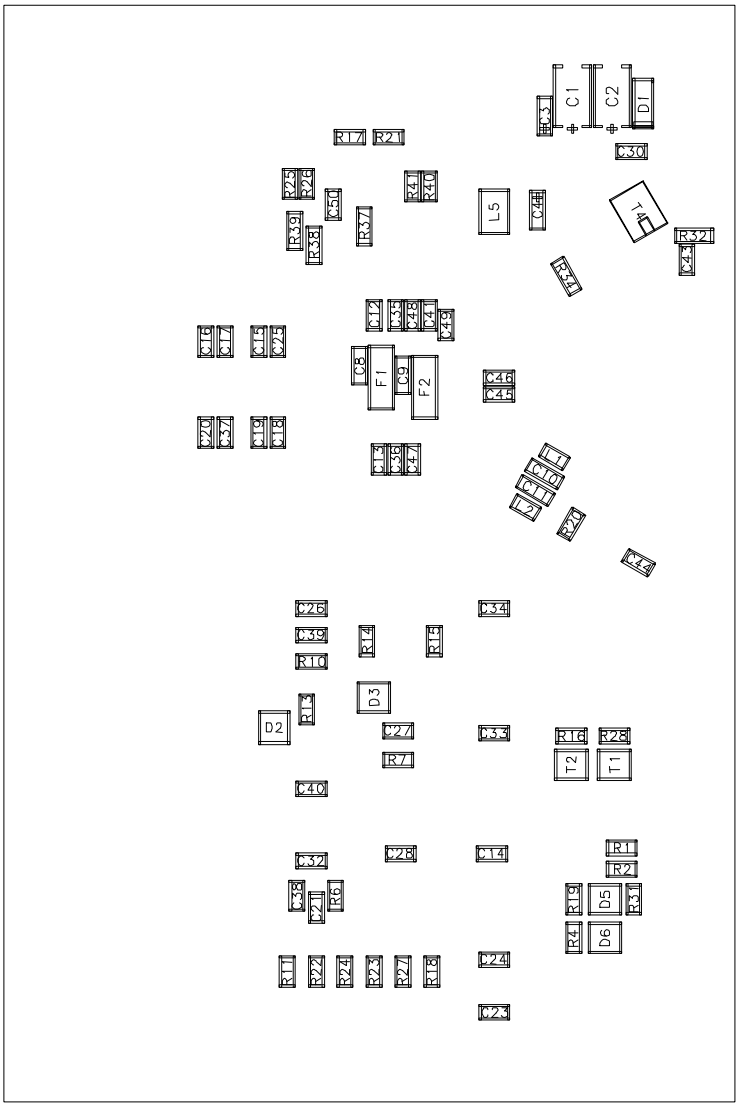
The list of components with their values and references is given from **Tables 2 to 6**. The list of components with their values and references for the examples of filter is given in **Table 7**.



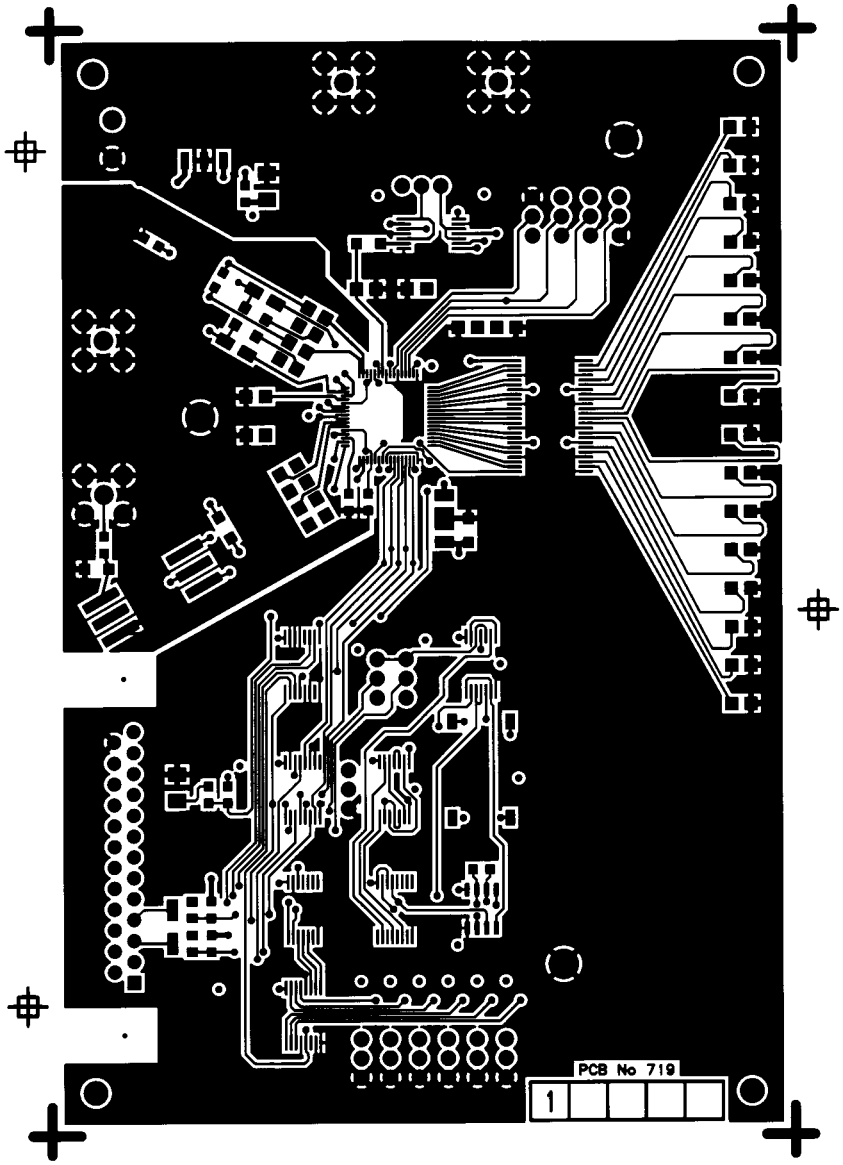
- Figure 29. Demoboard electrical diagram -



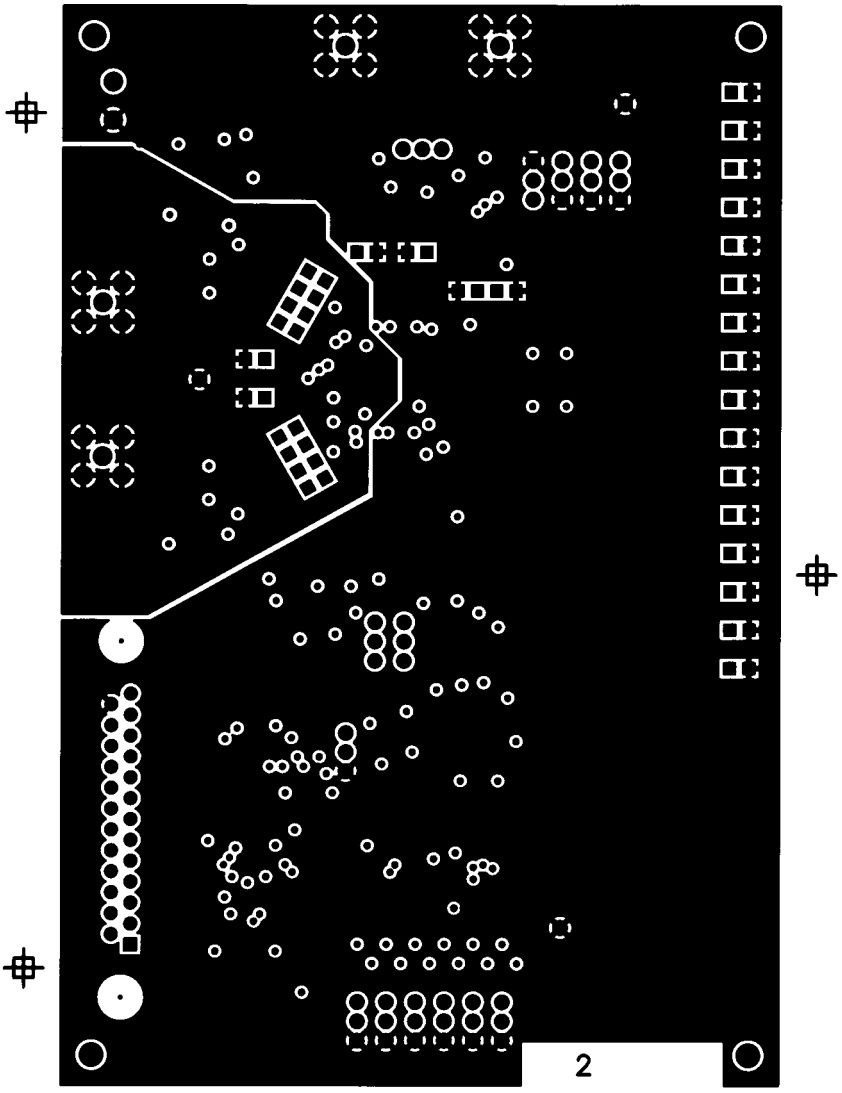
- Figure 30. Topside component implantation -



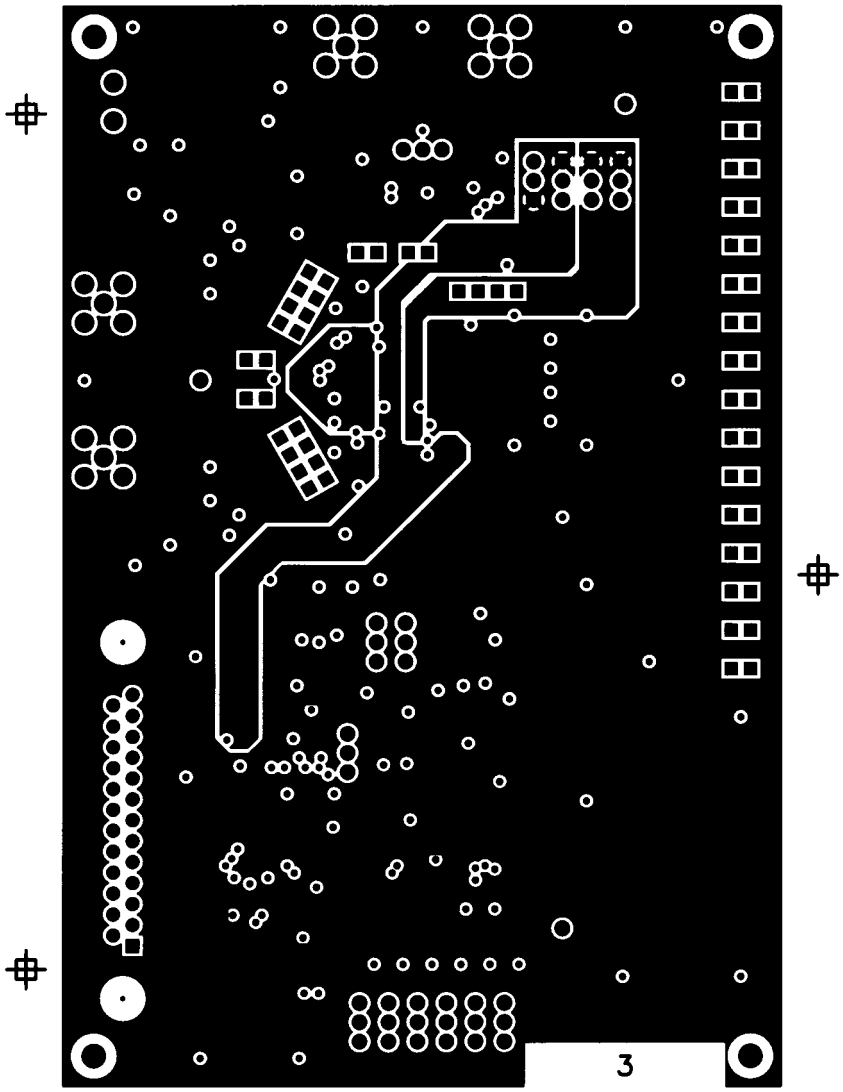
- Figure 31. Underside component implantation -



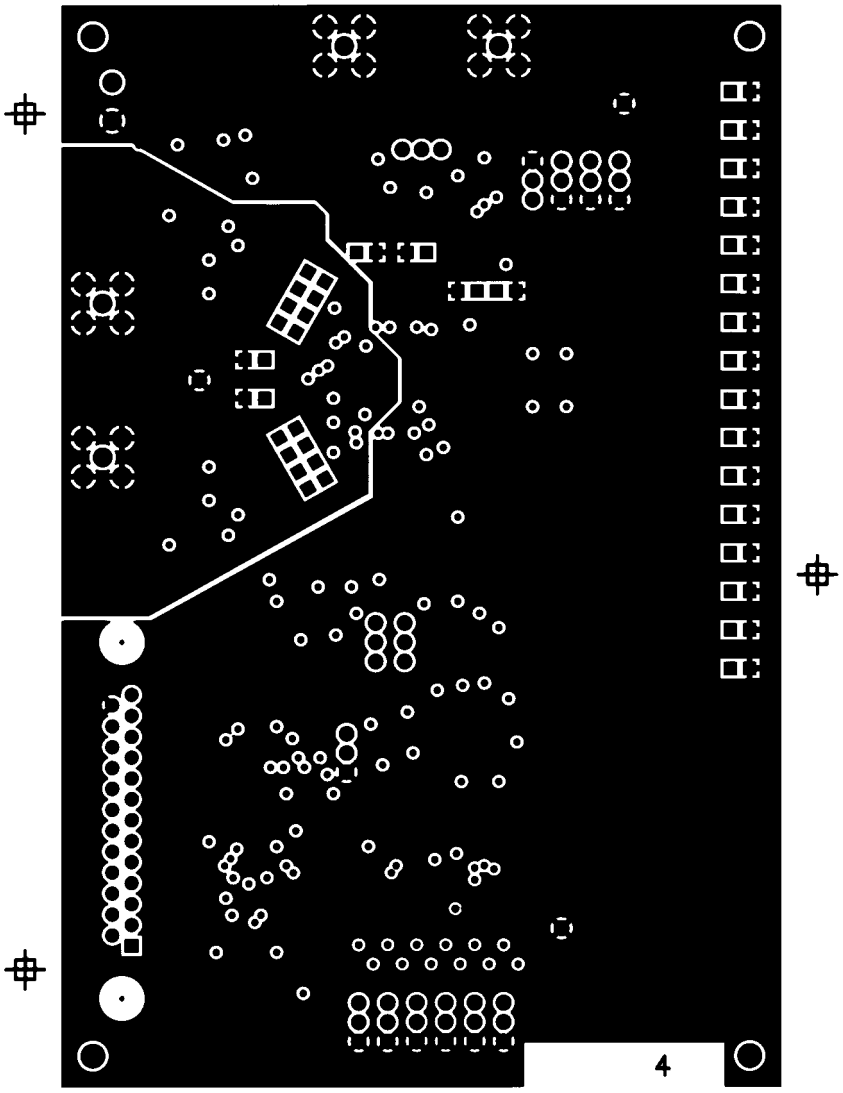
- Figure 32. Topside component layout (signal layer 1) -



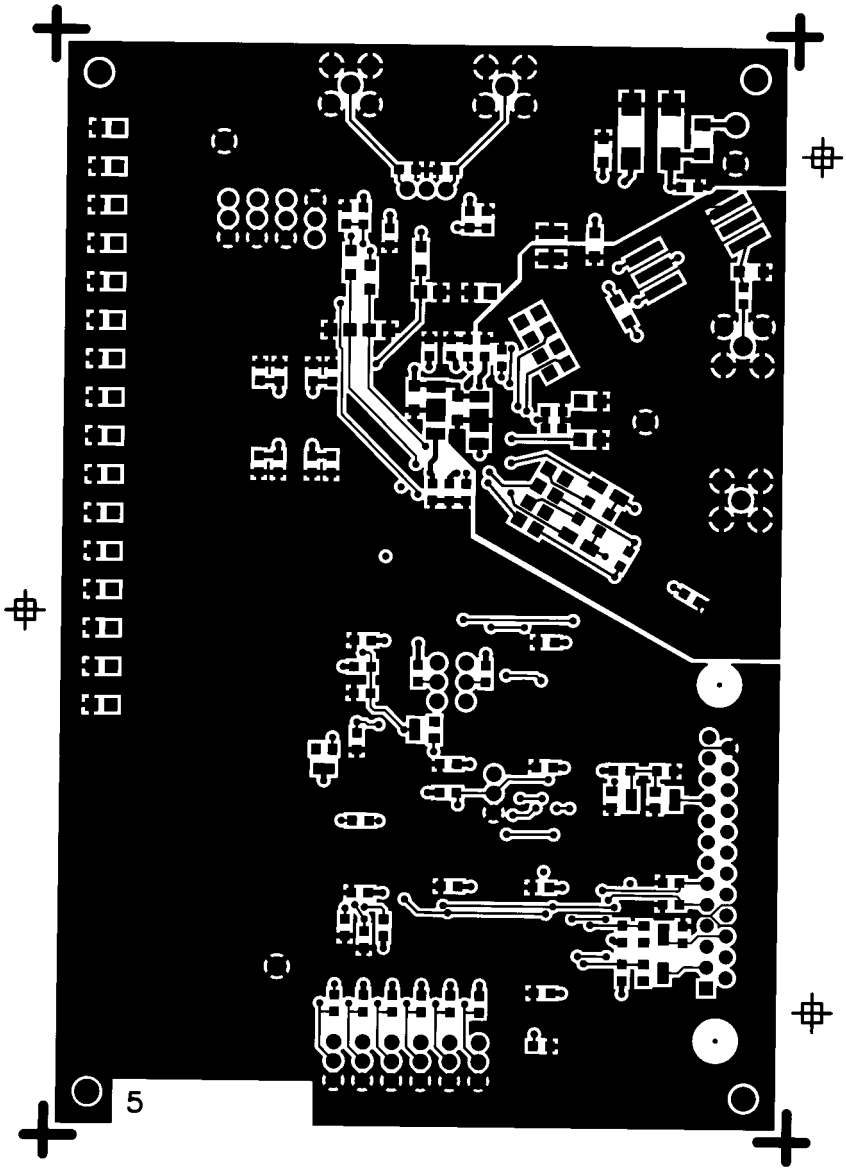
- Figure 33. Internal plane layout (ground layer 2) -



- Figure 34. Internal layout (supply layer 3) -



- Figure 35. Internal plane layout (ground layer 4) -



- Figure 36. Underside component layout (signal layer 5) -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C1	33µF/16V	CAPACITOR	293D/D	SPRAGUE
C2	22µF/16V	"	293D/D	"
C3	1µF/16V	"	293D/A	"
C4	1µF/16V	"	"	"
C5	330nF	‘	C1206	PHILIPS
C8	330nF	"	‘	‘
C9	330nF	"	‘	‘
C12	100nF	"	C0805	‘
C13	100nF	"	"	"
C14	100nF	"	"	"
C15	100nF	"	"	"
C16	100nF	"	"	"
C17	100nF	"	"	"
C18	100pF	"	‘	‘
C19	100nF	"	‘	"
C20	100nF	"	‘	"
C21	100nF	"	‘	"
C22	220nF	"	‘	"
C23	100nF	"	‘	"
C24	100nF	"	"	"
C25	100nF	"	"	"
C26	100nF	"	"	"
C27	100nF	"	"	"
C28	100nF	"	"	"
C29	10nF	"	"	"
C30	470nF	"	"	"
C31	68pF	"	"	"
C32	100nF	"	"	"
C33	100nF	"	"	"
C34	100nF	"	"	"
C35	100nF	"	"	"
C36	100nF	"	"	"
C37	100nF	"	"	"
C38	100nF	"	"	"
C39	100nF	"	"	"
C40	47pF	"	"	"
C41	100nF	"	"	"
C42	100nF	"	"	"
C43	220nF	‘	‘	‘
C44	10nF	"	"	"
C45	100nF	"	"	"
C46	100nF	"	"	"

- Table 2. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C47	100nF	CAPACITOR	C0805	PHILIPS
C48	100nF	"	"	"
C49	68pF	"	"	"
C50	100nF	"	"	"
C44	10nF	"	"	"
C44	10nF	"	"	"
C46	1µF/16V	"	‘	"
D1		DIODE	BYD17G	PHILIPS
D2		‘	BAS16	"
D3		‘	"	"
D4		‘	"	"
D5		‘	"	"
D6		‘	"	"
D7		‘	"	"
DS1		RED LED	LST 679-CO	SIEMENS
DS2		GREEN LED	LGT 679-CO	‘
F1	2nF	Π FILTER	4700-003-S	TUSONIX
F2	2nF	"	"	"
F3	2nF	"	"	"
IC1		EXCLUSIVE-OR	74LVT86DB	PHILIPS
IC2		D TYPE FLIP FLOP	74LVT16374ADL	‘
IC3		JOHNSON COUNTER	74HC4017DB	‘
IC4		BINARY RIPPLE COUNTER	74HC393DB	‘
IC5		2-INPUT MULTIPLEXER	74HC157DB	‘
IC6		‘	‘	‘
IC7		8-INPUT MULTIPLEXER	74HC151DB	‘
IC8		NOR	74HC02DB	‘
IC9		NAND	74HC00DB	‘
IC10		TIMER	TLC555CD	TEXAS INSTRUMENTS
IC11		LOW DROPOUT REGULATOR	LM3940	NATIONAL SEMI.
IC12		ADC	TDA8798HL	PHILIPS
J1	50Ω	CONNECTOR	SMA	RADIALL
J2		‘	‘	‘
J3	50Ω	CONNECTOR	SMA	RADIALL
J4	50Ω	"	‘	‘
J5		‘	MKSD	PHOENIX
J6		‘	SUB-D25 FEMALE	HARTING

- Table 3. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
K1		SWITCH	1C2P	SECME
K2		"	"	"
K3		"	"	"
K4		"	"	"
K5		"	"	"
K6		"	"	"
K7		"	"	"
K8		"	"	"
K9		"	"	"
K10		"	"	"
K11		"	"	"
K12		"	"	"
K13		"	"	"
K14		"	"	"
L1		HF70ACB-453215T	C1812	PHILIPS
R1	4.7KΩ	RESISTOR	0805	PHILIPS
R2	4.7KΩ	‘	‘	‘
R3	750Ω	‘	‘	‘
R4	4.7KΩ	‘	‘	‘
R5	4.7KΩ	‘	‘	‘
R6	680Ω	‘	‘	‘
R7	4.7KΩ	‘	‘	‘
R8	100Ω	‘	‘	‘
R9	4.7KΩ	"	"	"
R10	4.7KΩ	"	"	"
R11	4.7KΩ	"	"	"
R12	330Ω	"	"	"
R13	4.7KΩ	"	"	"
R14	4.7KΩ	"	"	"
R15	4.7KΩ	"	"	"
R16	3.3KΩ	"	"	"
R17	50Ω	"	"	"
R18	4.7KΩ	"	"	"
R19	20KΩ	"	"	"
R20	100Ω	‘	‘	‘
R21	50Ω	‘	‘	‘
R22	4.7KΩ	‘	‘	‘
R23	4.7KΩ	‘	‘	‘
R24	4.7KΩ	‘	‘	‘
R25	0Ω	‘	‘	‘

- Table 4. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
R26	**Do not solder**			
R27	4.7KΩ	RESISTOR	0805	PHILIPS
R28	4.7KΩ	‘	‘	‘
R29	4.7KΩ	‘	‘	‘
R30	750Ω	‘	‘	‘
R31	3.3KΩ	‘	‘	‘
R32	100Ω	‘	1206	‘
R33	100Ω	‘	‘	‘
R34	820Ω	‘	‘	‘
R35	820Ω	‘	‘	‘
R36	68Ω	‘	‘	‘
R37	56Ω	‘	‘	‘
R38	68Ω	‘	‘	‘
R39	56Ω	‘	‘	‘
R40	0Ω	‘	‘	‘
R37	**Do not solder**			
T1		TRANSISTOR	BC848B	PHILIPS
T2		‘	‘	‘
T3		RF TRANSFORMER	MCLT1-6T-KK81	MINI-CIRCUIT
T4		‘	‘	‘
BP1		PUSH BUTTON	3CSH9	MEC
TM1		MEASUREMENT POINT		COMATEL
TM2		‘		‘
TM4		‘		'
TP1		TEST POINT		COMATEL
TP2		'		‘
TP3		'		‘
TP4		‘		‘
TP5		'		‘
TP6		'		
TP7		'		'
TP8		'		'
TP9		'		'
TP10		'		'
TP11		'		'
TP12		'		'
TP13		'		'
TP14		'		'

- Table 5. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TP15		TEST POINT		COMATEL
TP16		"		"
TP17		"		"
TP18		"		"
TP19		"		"
TP20		"		"
TP21		"		"
TP22		"		"
TP23		"		"
TP24		"		"
TP25		"		"
TP26		"		"
TP27		"		"
TP28		"		"
TP29		"		"
TP30		"		"
TP31		"		"
TP32		"		"
TP33		"		"
TP34		"		"
TP35		"		"
TP36		"		"
TP37		"		"
TP38		"		"
TP39		"		"
TP40		"		"
TP41		"		"
TP42		"		"
TP43		"		"
TP44		"		"
TP45		"		"
TP46		"		"
TP47		"		"
TP48		"		"
TP49		"		"
TP50		"		"
TP51		"		"
TP52		"		"
TP53		"		"
TP54		"		"
TP55		"		"
TP56		"		"

- Table 5. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TP57		TEST POINT		COMATEL
TP58		"		"
TP59		"		"
TP60		"		"
TP61		"		"
TP62		"		"
TP63		"		"
TP64		"		"
TP65		"		"
TP66		"		"
TP67		"		"
TP68		"		"

- Table 6. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C6	100nF	CAPACITOR	C1206	PHILIPS
C7	100nF	"	"	"
C10	100nF	"	"	"
C11	100nF	"	"	"
L1	4.7µH	SELF	LQH1N220K04	MURATA
L2	4.7µH	"	"	"
L3	4.7µH	"	"	"
L4	4.7µH	"	"	"
R34	820Ω	RESISTOR	1206	PHILIPS
R35	820Ω	"	"	"

- Table 7. List of components for the filter -